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Performance of thermally deposited polycrystalline Ge-thin film transistors with a copper interlayer fabricated on glass substrates

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Abstract The performance of Ge- TFTs with a copper interlayer in the channel region is presented TFTs are fabricated in staggered electrode structure on perfectly cleaned glass substrates using thermal evaporation process with rare earth oxide Dy_2O_3 as gate insulator The TFTs are annealed at 370°C under high vacuum The TFTs exhibit a mobility of 0 646 $cm^2V^{-1}s^{-1}$ and threshold voltage of 3 V The characteristics and some electrical parameters of the TFTs with copper interlayer are evaluated using Weimer's model [*Phys Thin Films* **2** 149 (1964)] and characterized by Levinson *et al* [*J Appl Phys* **53** 1193 (1982)] model The various electrical parameters of the TFTs are compared with those of Ge - Dy_2O_3 TFTs fabricated without copper interlayer

Keywords Poly Ge-TFT, copper interlayer, Dy_2O_3

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1. Introduction

In large area electronics circuits, TFTs are widely used as driving devices. Especially in active matrix liquid crystal displays (AMLDs), TFTs are used as pixel transistors [1]. In the grain boundaries of a polycrystalline semiconductor, there are large numbers of defects due to incomplete atomic bonding or the dangling bonds due to which potential barriers are established in the grain boundaries .The grain boundary potential barriers in polycrystalline TFTs impede the motion of charge carriers from one crystallite to another and hence decrease the mobility [2]. The passivation of grain boundary states by atomic hydrogen is a well-established technique which is employed to reduce the grain boundary potential barrier in poly-Si [3]. It has been reported that, in polycrystalline Si, some of the dangling bonds in the grain boundaries can be completed by means of hydrogen passivation

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in which atomic hydrogen ties up with most of the dangling bonds and reduce the grain boundary potential barrier [4]. Copper passivation of dislocations in polycrystalline silicon reduces the potential barrier height at the grain boundaries [5].

Rare earth oxides play an important role in thin film transistors as gate insulators due to their high chemical stability, high dielectric constant and high resistivity [6-8].

Levinson *et al* [9] have proposed a model based on the grain boundary trapping for characterization of polycrystalline thin film transistors. Using this model the TFTs fabricated with a coper interlayer have been characterized and some important parameters such as trap density (N_t), critical donor density (N_d^*) and crystallite size (L) are evaluated These parameters are compared with the TFTs fabricated without copper interlayer.

2. Experimental details

2.1. Fabrication of the TFTs :

The TFTs were fabricated using thermal evaporation process in high vacuum better than $4x10^{-6}$ torr in staggered electrode structure on glass substrates. Aluminium was deposited first as source and drain electrodes. A channel of 50 μm length was produced with the help of a wire grill, fixed on the mask. A 1050Å channel layer was formed between the source-drain gap by deposition of Ge (510 Å), Cu (20 Å) and Ge (520 Å) layers in steps The Ge/Cu/Ge layers are deposited at substrate temperature of 250° C with a deposition rate of 0.5 $Å s^{-1}$. A layer of Dy_2O_3 of thickness 715 Å was deposited as gate insulator over the Ge/Cu/Ge layers. Finally, a layer of Al was deposited on the oxide layer as gate electrode. The fabricated TFTs were annealed in high vacuum at 370° C for 5 hours

Ge- Dy_2O_3 TFTs without copper interlayer have also been fabricated with the similar procedure as mentioned above. These TFTs are also annealed to a temperature of 370° C for 5 hours.

2.2. Measurements :

The film thicknesses were measured by multiple beam interference method. The resolution of the thickness measurement set-up is ± 10 Å. The gate capacitance was measured using auto computer LCR sortester (APLAB, Model 4912). The drain current, drain voltage were measured using the digital nanoammeters and digital multimeters.

3. Results and discussions

3.1. Electrical characteristics :

The characteristics depicting the variation of drain current (I_d) with drain voltage (V_d) at constant gate voltage (V_g) for the TFTs fabricated with a copper interlayer is shown in Figure 1. From Figure 1 it is noted that the TFTs with copper interlayer show well-modulated I_d *vs.* V_d characteristics at constant gate voltage (V_g). Figure 2 shows the field effect characteristics of the TFTs at drain voltage V_d = 8V.

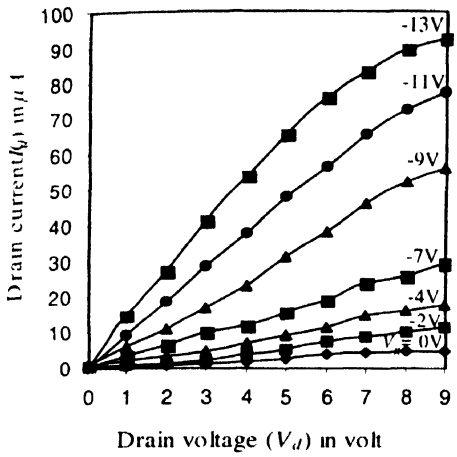

Figure 1. $I_d - V_d$ curves of the TFT's with copper interlayer

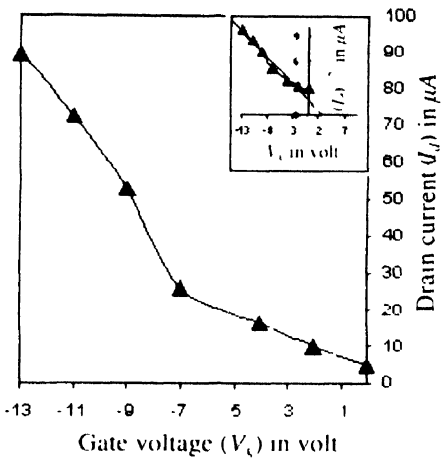

Figure 2. I_d - V_g curves of the TFT's with copper interlayer. The insert shows the variation of $\sqrt{I_d}$ at different V_d

The electrical parameters of TFTs are calculated using the following expressions [10]. Transconductance (g_m)

$$g_m = \left[\frac{\partial I_d}{\partial V_g}\right]_{V_d=const} = \frac{w}{l}\mu_{FET}C_{ox}V_d \tag{1}$$

where C_{ox} is the gate capacitance per unit area, w is the channel width, l is the channel length, V_d is the drain voltage and μ_{FET} is the field effect mobility.

Output drain resistance

$$r_d = \left.\frac{\partial V_d}{\partial I_d}\right|_{V_g=const} \tag{2}$$

amplification factor

$$\mu = g_m x r_d \tag{3}$$

and gain-bandwidth (*G.Bw*) product

$$G.Bw = \frac{g_m}{2\pi C_{ox}} . \tag{4}$$

The mobility of the devices is estimated using eq. (1). The calculated values of output drain resistance (r_d), transconductance (g_m), amplification factor (μ), mobility (μ_{FET}) and the gain-bandwidth product (*G.Bw*) of the TFTs are presented in Table 1.

Table 1 Comparison of some parameters of the TFTs with copper interlayer and without copper interlayer

Type of TFTs	Output resistance r_d (ohm)	Transconductance g_m (mho)	Amplification factor μ	Mobility μ_{FET} ($cm^2V^{-1}s^{-1}$)	Gain bandwidth product G Bw (KHz)
with copper interlayer	0 125 X 10^6	3 86 X 10^{-6}	0 49	0 646	1 31 X 10
without copper interlayer	89 29 X 10^6	0 0083 X 10^{-6}	0 70	1 44 X 10^3	9 35 X10

3 2 Characterization of the TFTs

The Ge semiconductor used in this investigation is polycrystalline in nature and usually contains many grain boundaries in the conducting channel, which interrupts the mean free path of the charge carriers and acts as trapping centers [11] Hence, grain boundary trapping model proposed by Levinson *et al* [9] is used to characterize the TFTs The expression for drain current I_d of the TFTs with polycrystalline materials is given by-

$$I_d = w\mu_b \frac{V_d}{l} C_{ox} V_g exp\left(\frac{-q^3 N_t^2 t}{8\varepsilon kTC_{ox}V_g} \right) \quad (5)$$

where, w is the channel width, l *is the* channel length, μ_b is the field effect mobility C is the insulator capacitance per unit area, N_t is the trap density per unit area and t is the thickness of the semiconductor film

From eq (5), it is evident that, the plot of ln (I_d/V_g) *vs* $(1/V_g)$ is a straight line (Figure 3) From the slope of this straight line, N_t can be estimated The deviation from linearity

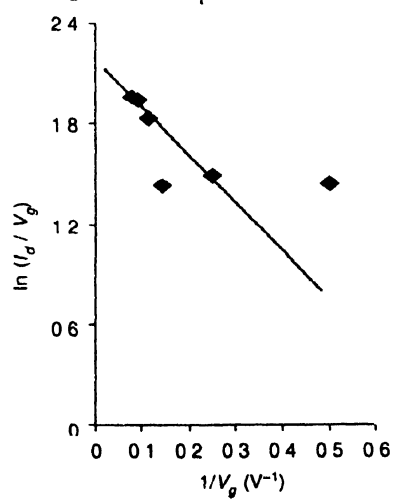

Figure 3. Plot of ln (I_d / V_g) *vs* $(1/ V_g)$ for Ge-Dy_2O_3 TFTs with a copper interlayer

in Figure 4 occurs, when $N_g/t = N_d^*$, where $N_g = (C_{ox}/q)\ V_g$ is the gate induced carrier concentration and N_d^* is the critical donor density The crystallite size L can be calculated from $N_d^* = N_t/L$ The values of N_t N_d^*, and L obtained for Ge-Dy_2O_3 TFTs with a copper interlayer are presented in Table 2

Table 2 Comparison of trap density (N_t), critical donor density (N_d) and crystallite size (L) of the fabricated devices with copper interlayer and without copper interlayer

Type of device	Trap density N_t (cm^{-2})	Critical donor density N_d (cm^{-3})	Crystallite size L (Å)
Ge Dy_2O_3 with copper interlayer	3 61 X 10^{11}	0 81 X 10^{17}	451 25
Ge Dy_2O_3 without Cu interlayer	1 86 X 10^{12}	1 61 X 10^{17}	121

3 3 Comparison of the parameters of the TFTs fabricated with copper interlayer and without copper interlayer

The drain current (I_d) *vs* drain voltage (V_d) characteristics of the TFTs, without copper interlayer are shown in Figure 4 Comparing Figures 1 and 4 it is seen that the family of drain current of the TFTs with copper interlayer exhibit higher drain current than the TFTs without copper interlayer This is due to their higher mobility and lower threshold voltage (V_T)

Figure 5 shows the field effect characteristics at drain voltage V_d = 8V for the TFTs without copper interlayer The threshold voltage (V_T) of the TFTs with copper interlayer and without copper interlayer have been evaluated by plotting $\sqrt{I_d}$ *vs* gate voltage (V_g) at constant drain voltage (V_d), which are shown in the insert of Figures 2 and 5, respectively, and are

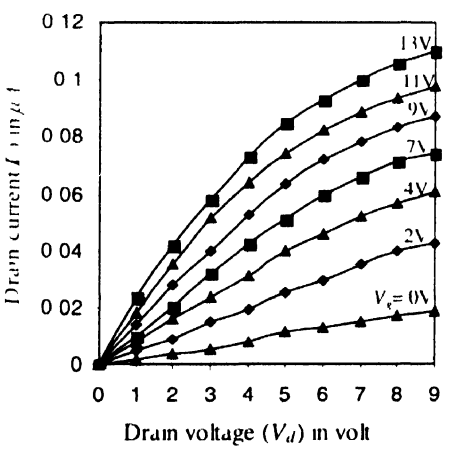

Figure 4. $I_d - V_d$ curves of the TFT's without copper interlayer

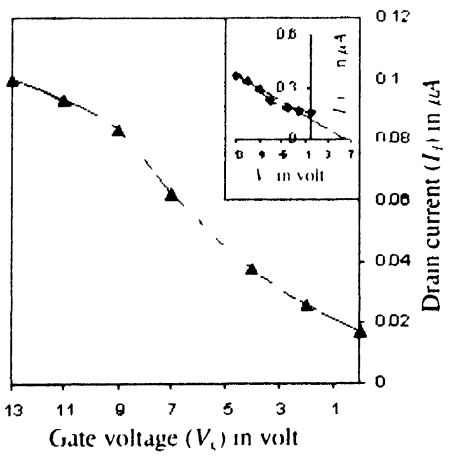

Figure 5. I_d - V_g curves of the TFT's without copper interlayer The insert shows variation of $\sqrt{I_d}$ at different V_g

found to be 3V for copper interlayer and 6V for without copper interlayer. The estimated values of the electrical parameters of the TFTs without copper interlayer are also presented in Table 1. The value of trap density (N_t), critical donor density (N_d^*) and crystallite size (L) of the TFTs without copper interlayer are also evaluated and these are presented in Table 2.

The mobility of TFTs with copper interlayer and without copper interlayer are found as 0.646 $cm^2V^{-1}s^{-1}$ and $0.4x10^{-3}$ $cm^2V^{-1}s^{-1}$ respectively which are shown in Table 1. The enhance mobility of the TFT's with copper interlayer is due to the fact that, during the heat treatment, the grain boundary states in the case of poly- Ge TFTs are passivated by copper in Ge. During the passivation, copper atom diffuses along the grain boundaries and completes some of the open bonds (dangling bonds). Consequently the interface states density drops and the potential barrier is lowered. The resulting effect is that the poly-Ge electrically progresses towards single crystal Ge characteristics, yielding higher mobility. The TFT without copper interlayer is also heated to the temperature 370° C, but it does not show enhance mobility as that of the TFT fabricated without copper interlayer. This implies that diffusion of Al in Ge does not take place though the TFTs are heated to a temperature of 370° C.

4. Conclusion

Comparing the characteristics and the electrical parameters it is seen that the performance of the TFTs fabricated with copper interlayer is better that than of the TFTs fabricated without copper interlayer. The TFTs with copper interlayer exhibit higher mobility than the TFTs without copper interlayer. It is observed that the threshold voltage (V_T) is significantly improved in case of TFTs with copper interlayer. The other electrical parameters such as output resistance (r_d), transconductance (g_m), trap density (N_t), critical donor density (N_d^*) and crystallite size (L) are also found to be better in case of TFTs with copper interlayer but amplification factors (μ) are comparable for both types of TFTs. From this observation it may also be concluded that TFTs with Dy_2O_3 could be realized.

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